REMARKS

This application was originally filed on 31 December 2003 with eighteen claims, three of which were written in independent form. Claims 1, 8, and 15 were amended on 16 February 2006. Claim 1 has been amended herein. Claims 15-18 have been allowed.

Claim 1:

Claim 1 was rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Application Publication No. 2004/0063595 to Park *et al.* ("Park").

Claim 1 has been amended to recite, "providing a wafer having an etched patterned layer and an overlying mask pattern resist." The applicant respectfully submits that the claim already recited a method of "removing pattern resist that remains after an etch of an underlying patterned layer" as stated in the preamble, the amendment should be considered non-narrowing.

Claim 1 recites "providing a wafer having an etched patterned layer and an overlying mask pattern resist; cleaning the wafer with a develop solution; ashing the surface of the wafer; and photochemically removing the pattern resist that remains after the cleaning and ashing steps."

The Examiner stated, Park discloses a method comprising the steps of "cleaning a semiconductor substrate/wafer with a chemical wet cleaning/develop solution (col 6, paragraph 0066, col 6, paragraph 0070)."

The applicant respectfully submits that the reference to paragraph 0066 appears to be in error as paragraph 0066 does not discuss wet cleaning or a develop solution, and is located on page 5 rather than page 6.

Park, in paragraph 0070 states, "The photoresist layer may be exposed by using a mask of a predetermined pattern and then developed to form photoresist patterns (step S20). The metallic layer may be etched (step S30) using the photoresist pattern as a mask, for example." Thus, Park is teaching developing the photoresist pattern, not "providing a wafer having an etched patterned layer and an overlying mask pattern" and "cleaning the wafer with a develop solution" as recited by Claim 1. As Park does not show, teach, or suggest the combination of limitations recited by Claim 1, the Examiner's rejection of Claim 1 as being anticipated by Park is unsupported by the

art and should be withdrawn.

Claims 2-7:

Claims 2 and 3 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Park in view of U.S. Patent Application Publication No. 2004/0053505A1 to Chinn *et al.* ("Chinn"). Claims 4, 5, and 7 were rejected under 35 U.S.C. § 102(e) as being anticipated by Park. Claim 6 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Park in view of U.S. Patent No. 6,472,315 to Nguyen *et al.* ("Nguyen").

Claims 2-7 depend from Claim 1 and should be deemed allowable for that reason, and on their own merits. For the reasons given above with respect to Claim 1, the Examiner has not presented a *prima facie* case of anticipation with respect to the limitations of Claim 1, much less a *prima facie* rejection with respect to the limitations of Claim 1 in combination with the additional limitations of the dependent claims. Furthermore, with respect to the combinations of prior art references used by the Examiner, the Examiner has not presented any teachings in the art that suggest the modification or combination proposed by the Examiner. The rejection of Claims 2-7 therefore is unsupported by the prior art and should be withdrawn.

Claim 8:

Claim 8 was rejected under 35 U.S.C. § 102(e) as being anticipated by Park.

Claim 8 has been amended to recite, "after said etching step" and "after said cleaning step" to clarify the order of the claimed steps.

Claim 8 recites, "etching the resist material and the material for the patterned layer; cleaning the resist material and remaining material for the patterned layer with a develop solution after said etching step; ashing the surface of the wafer after said cleaning step; and photochemically removing the pattern resist that remains after the cleaning and ashing steps."

The Examiner stated, Park discloses a method comprising the steps of "cleaning a semiconductor substrate/wafer with a chemical wet cleaning/develop solution (col 6, paragraph 0066, col 6, paragraph 0070)."

The applicant respectfully submits that the reference to paragraph 0066 appears to be in

error as paragraph 0066 does not discuss wet cleaning or a develop solution, and is located on page 5 rather than page 6.

Park, in paragraph 0070 states, "The photoresist layer may be exposed by using a mask of a predetermined pattern and then developed to form photoresist patterns (step S20). The metallic layer may be etched (step S30) using the photoresist pattern as a mask, for example." Thus, Park is teaching developing the photoresist pattern, not "cleaning the resist material and remaining material for the patterned layer with a develop solution after said etching step" as recited by Claim 8. As Park does not show, teach, or suggest the combination of limitations recited by Claim 8, the Examiner's rejection of Claim 8 as being anticipated by Park is unsupported by the art and should be withdrawn.

Claim 8 additionally recites, "ashing the surface of the wafer after said cleaning step; and photochemically removing the pattern resist that remains after the cleaning and ashing steps." Park does not show, teach, or suggest this series of cleaning, ashing, and photochemically removing steps following an etch step.

Claims 9-14:

Claims 9 and 10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Park in view of Chinn. Claims 11, 12, and 14 were rejected under 35 U.S.C. § 102(e) as being anticipated by Park. Claim 13 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Park in view of U.S. Patent No. 6,472,315 to Nguyen *et al.* ("Nguyen").

Claims 9-14 depend from Claim 8 and should be deemed allowable for that reason, and on their own merits. For the reasons given above with respect to Claim 8, the Examiner has not presented a *prima facie* case of anticipation with respect to the limitations of Claim 8, much less a *prima facie* rejection with respect to the limitations of Claim 8 in combination with the additional limitations of the dependent claims. Furthermore, with respect to the combinations of prior art references used by the Examiner, the Examiner has not presented any teachings in the art that suggest the modification or combination proposed by the Examiner. The rejection of Claims 9-14 therefore is unsupported by the prior art and should be withdrawn.

In view of the amendments and the remarks presented herewith, it is believed that the

claims currently in the application accord with the requirements of 35 U.S.C. § 112 and are allowable over the prior art of record. Therefore, it is urged that the pending claims are in condition for allowance. Reconsideration of the present application is respectfully requested.

Respectfully submitted,

Charles A. Brill
Reg. No. 37,786

Texas Instruments Incorporated
PO Box 655474 M/S 3999
Dallas, TX 75265
(972) 917-4379
FAX: (972) 917-4418